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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/038,431	12/31/2001	Sushma Shrikant Trivedi	04860.P2687	7868

7590 02/09/2005

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/038,431	TRIVEDI ET AL.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-18,20-32 and 34-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-18,20-32 and 34-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-7, 9-18, 20-32, and 34-36 and new claims 37-39 have been examined. Claims 1, 4-7, 9, 12, 15-18, 20, 23, 26, 29-32, and 34 have been amended as per Applicant's request. New claims 37-39 have been added as per Applicant's request. Claims 8, 19, and 33 have been cancelled as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Amendment as received on 15 November 2005 and IDS as received on 15 November 2004.

Information Disclosure Statement

3. Applicant discloses a list of related applications and they have been considered. However, it is unclear whether or not the Applicant wishes this list of related applications to be cited should this case be allowed and the application published. Please clarify.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-7, 9-18, 20-32, and 34-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chehrazi et al., U.S. Patent No. 6,282,556 (herein referred to as Chehrazi) in view of Mennemeier et al., U.S. Patent No. 6,036,350 (herein referred to as Mennemeier).

6. Regarding claims 1, 12, 23 and 26, taking claim 1 as exemplary, Chehrazi has taught a method for execution by a microprocessor in response to receiving a single instruction (Chehrazi Col.20 lines 42-52), the method comprising:

a. Receiving a first plurality of numbers (Chehrazi 310 of Fig.20B, Col.20 line 62 – Col.21 line 1) and a second plurality of numbers (Chehrazi 312 of Fig.20B, Col.20 line 62 – Col.21 line 1),

b. Generating a third plurality of numbers, each of which is an absolute difference between a number in the first plurality of numbers and a number in the second plurality of numbers (Chehrazi Col.21 lines 6-12),

c. Wherein the sum of third plurality of numbers are saved in an entry in a register file (Chehrazi Col.20 lines 47-58),

d. Wherein the above operations are performed in response to the microprocessor receiving the single instruction (Chehrazi Col.20 lines 42-52, 61-62).

7. Chehrazi has not explicitly taught wherein the third plurality of numbers themselves are saved in an entry in a register file. However, Mennemeier has taught storing a third plurality of numbers, specifically a vector of absolute differences, in a instruction specified register (Mennemeier, Col.7 line 64 – Col.8 line 23) so that the absolute differences can be used in other operations that require the distance assessment that the results represent (Mennemeier, Col.8 line 21-23). One of ordinary skill in the art would have recognized that it is desirable to retain results that will be used by future instructions so that the results don't need to be recalculated. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Chehrazi to store the absolute differences, rather than the sum of the absolute differences, in an

instruction specified register so that the values could be reused by other operations that require the data, thus improving throughput by avoiding the recalculation of the data.

8. Claims 12, 23, and 26 are nearly identical to claim 1. However, Chehrazi has taught the differences. Claim 12 differs in the claim being comprised within a machine-readable media (Chehrazi Col.20 lines 42-46), while claims 23 and 26 differs in the claims being comprised within an execution unit (Chehrazi Col.7 lines 20-40). Also, claim 23 claims wherein the microprocessor is a media processor disposed on an integrated circuit with a memory controller (Chehrazi column 5, lines 43-54). Besides these differences, the claims encompass the same scope as claim 1. Thus, claims 12, 23 and 26 are rejected for the same reasons as claim 1.

9. Regarding claims 2, 13, 24 and 27, taking claim 2 as exemplary, Chehrazi has taught a method as in claim 1, wherein an absolute difference between a first number and a second number is computed using a method comprising:

a. Producing a first intermediate number by subtracting the second number from the first number (Chehrazi Col.21 lines 1-8),

b. Producing a second intermediate number by subtracting the first number from the second number (Chehrazi Col.21 lines 1-8),

c. Selecting a positive number from the first intermediate number and the second intermediate number as the absolute difference between the first number and the second number (Chehrazi Col.21 lines 8-12),

d. Wherein the microprocessor is a media processor (Chehrazi 108 of Fig.1, Col.3 lines 6-7) disposed on an integrated circuit with a memory controller (Chehrazi 100 of Fig.1, Col.5 lines 46-54).

10. Claims 13, 24 and 27 are nearly identical to claim 2. Claim 13 lacks the recitation of a media processor disposed on an integrated circuit with a memory controller, and claims 13, 24 and 27 differ in their parent claims, but encompass the same scope as claim 2. Thus, claims 13, 24 and 27 are rejected for the same reasons as claim 2.

11. Regarding claims 3, 14 and 28, taking claim 3 as exemplary, Chehrazi has taught a method as in claim 2, wherein the first intermediate number and the second intermediate number are produced in parallel (Chehrazi Col.21 lines 1-8), and wherein the third plurality of numbers are generated substantially simultaneously (Chehrazi Col.21 lines 8-12).

12. Claims 14 and 28 are nearly identical to claim 3, both differing in their lack of having the third plurality of numbers being generated substantially simultaneously, as well as differing in their parent claims, but both encompass the same scope as claim 3. Thus, Claims 14 and 28 are rejected for the same reasons as claim 3.

13. Regarding claims 4, 15 and 29, taking claim 4 as exemplary, Chehrazi has taught a method as in claim 2, further comprising:

a. Testing if an overflow occurs in producing the first intermediate number and the second intermediate number (Chehrazi Col.20 lines 9-18),

b. Saturating the absolute difference between the first number and the second number if an overflow occurs (Chehrazi Col.20 lines 9-18).

14. Here, because the SABD instruction is a packed instruction (Chehrazi Col.20 lines 54-55), if overflow on subtraction operations is detected, saturation is performed on the result of the subtraction (Chehrazi Col.20 lines 9-18).

15. Claims 15 and 29 are nearly identical to claim 4, differing in their parent claims, but encompassing the same scope as claim 4. Thus, claims 15 and 29 are rejected for the same reasons as claim 4.

16. Regarding claims 5, 16 and 30, taking claim 5 as exemplary, Chehrazi has taught a method as in claim 1, wherein the first plurality of numbers are received from a first entry in the register file (Chehrazi Col.20 lines 47-58).

17. Claims 16 and 30 are nearly identical to claim 5, differing in their parent claims, but encompassing the same scope as claim 5. Thus, claims 16 and 30 are rejected for the same reasons as claim 5.

18. Regarding claims 6, 17 and 31, taking claim 6 as exemplary, Chehrazi has taught a method as in claim 5, wherein the single instruction specifies a way to partition a string of bits in the first entry into a first plurality of numbers (Chehrazi Col.20 lines 61-65). Here, the SABD instruction specifies a register in the register file, which corresponds to the plurality of numbers, and specifies that the data in the register be interpreted to be 16 separate 8-bit numbers.

19. Claims 17 and 31 are nearly identical to claim 6, differing in their parent claims, but encompassing the same scope as claim 6. Thus, claims 17 and 31 are rejected for the same reasons as claim 6.

20. Regarding claims 7, 18 and 32, taking claim 7 as exemplary, Chehrazi has taught a method as in claim 5, wherein the single instruction specifies an index of the entry in the first register file (Chehrazi 560c and 560d of Fig.20a, Col.20 lines 47-58).

21. Claims 18 and 32 are nearly identical to claim 7, differing in their parent claims, but encompassing the same scope as claim 7. Thus, claims 18 and 32 are rejected for the same reasons as claim 7.

22. Regarding claims 9, 20 and 34, taking claim 9 as exemplary, Chehrazi in view of Mennemeier has taught a method as in claim 1, wherein the single instruction specifies an index of the entry in a the register file (Mennemeier, Col.7 line 64 – Col.8 line 23, as well as above paragraph 39).

23. Claims 20 and 34 are nearly identical to claim 9, differing in their parent claims, but encompassing the same scope as claim 9. Thus, claims 20 and 34 are rejected for the same reasons as claim 9.

24. Regarding claims 10, 21 and 35, taking claim 10 as exemplary, Chehrazi has taught a method as in claim 1, wherein a type of each of the first and second pluralities of numbers is one of:

a. Unsigned integer (Chehrazi Col.20 lines 54-55),

b. Signed integer (Chehrazi Col.20 lines 54-55),

c. Floating point number.

25. Here, because the claim is written in the alternative format, only one of the three possible limitations is required to be met. Thus, Chehrazi has taught the limitations of claim 10.

26. Claims 21 and 35 are nearly identical to claim 10, differing in their parent claims, but encompassing the same scope as claim 10. Thus, claims 21 and 35 are rejected for the same reasons as claim 10.

27. Regarding claim 11, 22 and 36, taking claim 11 as exemplary, Chehrazi has taught a method as in claim 1, wherein a size of each of the first and second pluralities of numbers is one of:

a. 8 bits (Chehrazi Col.20 lines 61-65),

b. 16 bits,

c. 32 bits.

28. Here, because the claim is written in the alternative format, only one of the three possible limitations is required to be met. Thus, Chehrazi has taught the limitations of claim 11.

29. Claims 22 and 36 are nearly identical to claim 11, differing in their parent claims, but encompassing the same scope as claim 11. Thus, claims 22 and 36 are rejected for the same reasons as claim 11.

30. Regarding claim 25, Chehrazi has taught a processing system comprising an execution unit as in claim 23 (Chehrazi Fig.1).

31. Regardin claim 37, Chehrazi has taught wherein a type of each of the first and second pluralities of numbers is floating point number (Chehraze column 1, lines 19-21 and column 9, lines 37-41).

32. Regarding claim 38, Chehrazi has taught wherein the microprocessor is a media processor disposed on an integrated circuit with a memory controller (Chehrazi column 5, lines 43-54).

33. Regarding claim 39, Chehrazi has taught means for testing is an overflow occurs (Chehrazi Col.20 lines 9-18).

Response to Arguments

34. Applicant's arguments with respect to claims 37-39 have been considered but are moot in view of the new ground(s) of rejection.

35. Applicant's arguments filed 24 November 2004 with regards to claims 1-36 have been fully considered but they are not persuasive.

36. Applicant argues in essence on page 12 "Thus, no single instruction of Chehrazi computes a vector of absolute differences and outputs the vector of absolute differences in an entry of a register file." This has not been found persuasive. The vector of absolute differences was taught not by Chehrazi but by Mennemeier. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

37. Applicant argues in essence on page 12 "Thus, Mennemeier uses an instruction set very different from Chehrazi." The instruction set relied upon was that taught by Chehrazi not Mennemeier, and the instruction set in Mennemeier has no bearing on the rejection, since it was relied upon to teach the limitation of saving the third plurality of numbers in an entry in a register file, not the instruction set. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

38. Applicant argues in essence on page 13

> When viewed together, Chehrazi and Mennemeier show no indication of an arrangement in which a single instruction is used to compute and output absolute differences. Chehrazi showing a sum of absolute differences instruction that does not output absolute differences is a clear indication of non-obviousness.

39. This has not been found persuasive. A test of whether a combination is feasible is not whether a device will work or not by taking the entire invention of the secondary reference and forcing it to work in the device of the primary reference, but whether the feature(s) cited and taught in the secondary reference is combinable with the primary reference. In this case, the only portion of Mennemeier relied upon was that the absolute difference results, instead of being summed as taught by Chehrazi, is outputted to a register file. In response to applicant's argument above, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

40. Applicant argues in essence on page 14 "There is no indication that media coprocessor unit (108) is on an integrated circuit ***with a memory controller***." This has not been found persuasive. The memory controller is inherent to the media coprocessor, since the only way for the processor to function properly with the memory is through a memory controller. Memory controllers are an inherent part of a processor, since it is what controls the transfer of data between memory and the execution area or peripheral devices. Please see the FOLDOC definition of processor.

41. Applicant argues in essence on page 14 "In fact, a person skilled in the art can clearly see that the SABD instruction is not one of these Pack instructions." This has not been found persuasive. The Pack instruction description was used to show that there is overflow checking and saturation is performed within the system. In actuality, the adder-subtractor where the SABD instruction is performed treats all the instructions it executes as packed instructions, since it automatically performs saturation when add or subtract operations are not within the required range, i.e. underflow or overflow occurs (Chehrazi column 13, lines 15-16).

Conclusion

42. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

43. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

44. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

45. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

46. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
3 February 2005

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